

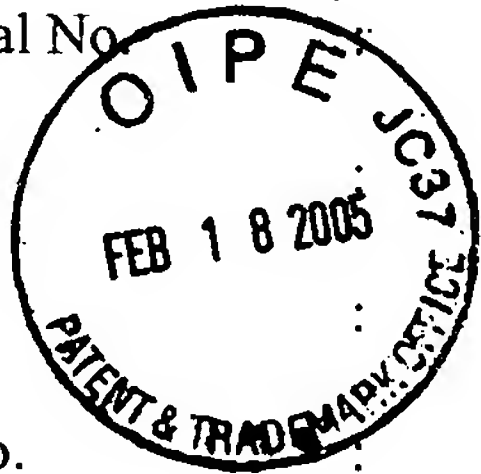
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DOCKET NO.: 03-LJ-011 (STMI01-03011)  
Customer No.: 30425

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : Razak Hossain  
U.S. Serial No. : 10/604,964  
Filed : August 28, 2003  
For : SCAN CHAIN MODIFICATION FOR REDUCED LEAKAGE  
Group No. : 2812  
Examiner : (Not Yet Assigned)



MAIL STOP AMENDMENT

Commissioner of Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

Sir:

The undersigned hereby certifies that the following documents:

1. Information Disclosure Statement;
2. Form PTO/SB/08B;
3. Copy of the European Search Report issued in related European Patent Application No. 04255064.0;
4. Four (4) references as cited on Information Disclosure Statement; and
5. A postcard receipt;

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on Feb 15, 2005.

Date: Feb 15, 2005

Kathy Hamilton  
Mailer

Date: Feb. 18, 2005

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**INFORMATION DISCLOSURE STATEMENT**

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents, publications and other information herein are listed below and on the attached Form PTO/SB/08B. These references were located in an International/European (choose one) Search Report issued in the related European Patent Application No. 04255064.0, a copy of which is attached hereto. Copies of the listed references are submitted herewith.

**Publications**

ABDOLLAHI, A., et al., "Leakage Current Reduction in Sequential Circuits by Modifying the Scan Chains," XP002306227, March 24, 2003, Proceedings of the Fourth International Symposium on Quality Electronic Design, IEEE Computer Society, pages 49-54.

SANKARALINGAM, R., et al., "Reducing Test Power During Test Using Programmable Scan Chain Disable," XP010587990, Proceedings of the First IEEE International Workshop on Electronic Design, Test and Applications, January 29, 2002, pages 159-163.

WANG, S., "Generation of Low Power Dissipation and High Fault Coverage Patterns for Scan-Based BIST," XP010609814, ITC International Test Conference, Paper 29.3, Oct. 7-10, 2002, pages 834-843.

SINANOGLU, O., et al, "Test Power Reduction Through Minimization of Scan Chain Transitions," XP-002306228, Proceedings of the 20<sup>th</sup> IEEE VLSI Test Symposium, April 28, 2002, pages 166-171.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement.


In accordance with 37 C.F.R. 1.97(e), the undersigned certifies that each item of information contained in the Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Information Disclosure Statement.

Further, pursuant to 37 C.F.R. § 1.97(e) and the above statements, no fee is believed to be due for the filing of this Information Disclosure Statement.

Respectfully submitted,

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